

APS Scientific Computation Seminar Series

Speaker: Yatish Kumar
ESnet Affiliate

Title: FPGA Acceleration for Data Scientists and Network Engineers

Date: Monday, August 17, 2020

Time: 1:00 p.m.

Location: <https://bluejeans.com/929021047>

Hosts: Nicholas Schwarz, Mathew Cherukara, and Antonino Miceli

Abstract:

FPGAs come with a steep learning curve, and assumption that the user is knowledgeable and trained as a Digital ASIC developer. This barrier to entry is being tackled using two different approaches: 1) High Level Synthesis where a user programs in a language like OpenCL and the hardware is automatically generated and 2) Overlay processors, where a team of hardware designers build a domain specific processor on the FPGA, and present it to the user for programming in a domain specific language for DSP / Networking etc... This talk will discuss the work being done at ESnet and LBNL-Computer Architecture Group on Overlay Processors, drawing on examples from an overlay Network Processor, as well as an overlay DSP processor. Simple tooling using Python and Jupyter notebooks is all that is assumed on the part of the Data Scientists from ALS and NCEM to interact with the FPGA design team. A cluster with 48 FPGA cards will be made available for all interested users at APS to experiment with both HLS and Overlays.